Roy Szweda

From the production viewpoint, the need is for more efficient processes with higher yield and hence lower unit cost. This is especially true as markets begin to pick up. It applies equally to micro as well as opto-electronic devices. Another interesting factor is the incorporation of MEMS functions in small-scale integrated circuits. In this article some new developments in GaN, InP, SiC and others will be highlighted.

Etch processes support III-Vs market expansion

With the III-Vs business only now emerging from troubled times, equipment sales for R&D and production are picking up. Previously, not only were no fabs being built, but also fab closures meant a bloated second-hand market. Sadly, some equipment was being auctioned off still in the delivery crates. "The business is now facing better times with the many challenges and opportunities that an upturn may bring," says Wyn Meredith of Compound Semiconductor Technologies (CST). "If demand picks up quickly, then equipment makers must provide the tools best matched to the market. For some suppliers this will mean going from an almost idle state to full throttle. It should be an interesting time for all."

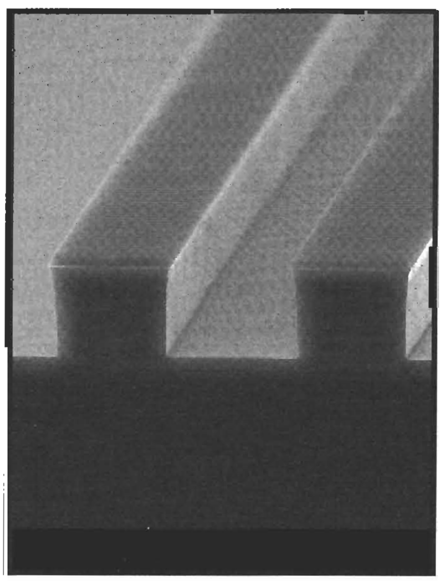


Figure 1. Compound Semiconductor Technologies prefers ICP for waveguide fabrication.

The etch market for compound semiconductors is served by a handful of equipment vendors. These have remained basically the same since our previous report: OIPT, STS, Tegal, Temescal, Trikon and Unaxis; there are no new etch start-ups, and while the familiar company names are still here, many staff changes have taken place. That is not unexpected, since the industry is well known for personnel transfers, said one respondent who could speak from experience. However, fairly high numbers have left the business to pursue other careers. In due course it is not unlikely that some will return to their former employ, as it becomes a matter of all hands to the pumps.

Reactive Ion Etching

One of the key etch processes for III-Vs remains RIE. As Dr Giuliana Morello of the Agilent Technologies labs in Italy says, RIE is the most used technique for optoelectronic devices. "This is because of its good factors such as anisotropy, reproducibility and uniformity. But RIE induces a damage layer which can degrade optical performance and reliability. Like others we have been evaluating the characteristics for etching InP.

"The damage changes the conductivity so naturally our approach involves comparing the conductance of the material before and after etching. This has enabled us to better optimise the RIE for such structures as the grating for DFB lasers and mesa etching."

GaN-based semiconductors are very attractive materials for use in optoelectronic devices, such as light emitting diodes and laser diodes, and for developing high power devices. In order to fabricate GaN-based devices successfully, high etch rates, high etch selectivities, vertical etch profiles, and smooth sidewalls are required in the dry etching process. In general, chlorine-based plasmas have been used to obtain high etch rates and vertical etch profiles in the GaN etch processes.

Dave Barrow, CST, commented on the advantages of RIE for manufacturing processes for both InP and GaAs structures. "We find that methane-hydrogen RIE gives us the fine etch rate control required for shallow etching structures such as DFB gratings, buried heterostructure mesas etc. The uniformity of the sidewall profile that can be achieved is pretty impressive when using a well characterised etch process. Polymer formation and sidewall damage can be a concern, but can be minimised by employing additional etching techniques post RIE."

"However for applications requiring deep etching (>5 microns) eg. AWG's, Echelle gratings, we prefer ICP (see Figure 1). It offers a flexible etch chemistry which allows us to optimise processes for a wide range of quaternary systems. We find it particularly useful for the fine optimisation of waveguide profiles required for multi-overgrowth integration schemes. Creating a defect free, continuous active-passive interface is the key to improving device performance.

"Our customers are demanding more sophisticated etching solutions as the complexity and density of photonic device designs increases, so we have to respond by continually developing both platforms."

Inductively-coupled plasma

However, another key technique is ICP, which is now being applied to the demanding task of SiC and III-nitride device processing. For example, R W Martin and his colleagues at the Department of Physics and Applied Physics, University of Strathclyde have collaborated with the Dept of Materials Science and Engineering, University of California, Berkeley, to investigate GaN microcavities, formed by a novel laser lift-off and plasma etching approach.

They used PL measurements to investigate GaN microcavities formed between two all-oxide distributed Bragg reflectors. The structures are fabricated using a combination of laser lift-off to separate MOVPE-grown epitaxial GaN layers from their sapphire substrates, inductively coupled plasma etching to thin the GaN and electron-beam evaporation to deposit silica/zirconia multilayer mirrors. The first mirror is deposited on the as-grown GaN surface, before bonding to a silicon substrate for the laser lift-off process, which uses a 248nm KrF laser to selectively decompose GaN at the GaN/sapphire interface.

The second dielectric mirror is deposited on the GaN surface exposed by the substrate removal, in some cases following an etch-back stage. This etch-back, achieved using ICP and wet chemical etching, removes the low-quality GaN nucleation layer. It also controls the cavity length and modification of the exposed surface. Our PL measurements have shown cavity-filtered luminescence from both etched and non-etched microcavities." says Dr Martin. "Analysis of the observed modes gives cavity finesses of approximately 10 for 2.0 and 0.8m GaN cavities fabricated from the same wafer, indicating that the etch-back has had little effect on microcavity quality."

The fabrication of AlGaInAs and GaInAsP buried heterostructure lasers by in situ etching has been described by E Veuhoff and colleagues at Infineon Technologies AG, Munich, Germany. The team's approach uses tertiarybutyl chloride (TBCl). TBC pyrolyses without forming side products that might inhibit the etching process. Furthermore, representing a starting substance in the production of arsine and TBA, it is claimed to be available in high purity. A good long-term stability is also anticipated.

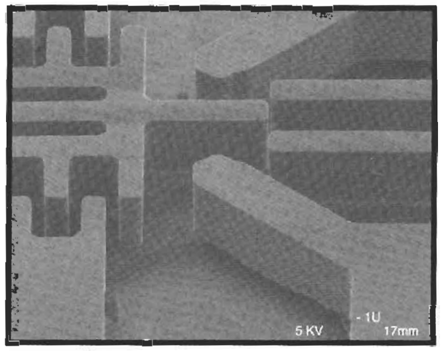
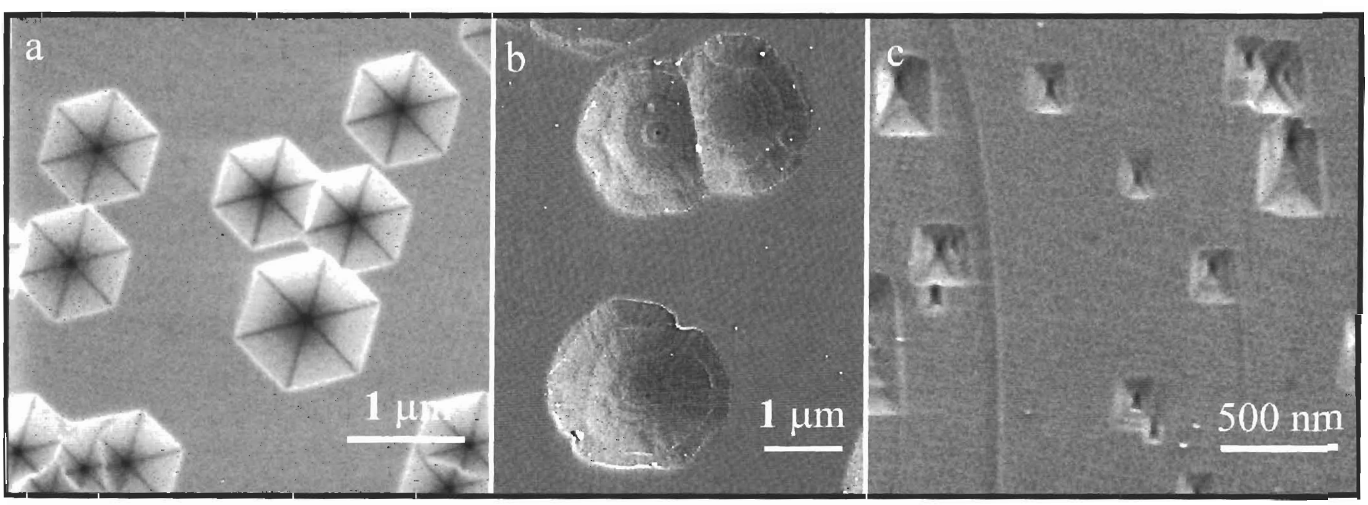


Figure 2: III-V MEMS Devices at Sandia National Laboratories. SEM photograph of GaAs/AlGaAs cantilever switch fabricated by RIBE.

"We chose this because it allows etching of both GaInAsP/InP and AlGaInAs/InP structures. This novel precursor is less corrosive and available in highest purity. It is proving suitable for the fabrication of BH lasers in our MOVPE system. Thus after in-situ etching of the laser ridge overgrowth of the structure can subsequently be performed in the same MOVPE system without exposing the sensitive AL containing MQW structure to air, ensuring improved long term device stability."

InP etching

As previously mentioned, wet processing of III-V structures is also important. For example, Xin Cao at the Ultrafast Systems Group, Dept of Electronics & Electrical Engineering, University of Glasgow, has been developing a new non-selective wet digital etching tech-



SEM image of etch pits formed on Ga- (a) and N- polar (b) {0001} planes and on (100) GaN cleavage plane (c) of high defect-density GaN epilayers. "Defect-selective etching is a fast and simple way to determine density and distribution of defects in semiconductor single crystals, epilayers and devices," says Grzegorz Kamler from the High Pressure Research Center, Polish Academy of Sciences, which is shortly to publish results of a collaborative project with the University of Nijmegen and Warsaw University of Technology (European Physical Journal - Applied Physics). "As far as I know it is the first attempt of etching of GaN planes different than (0001) and we have studied the effect of molten E+M etch on MOCVD-, MBE- and HVPE-grown epilayers and LD and LED structures."

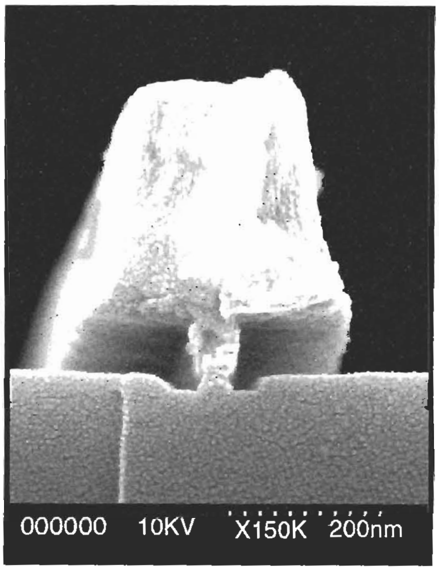


Figure 4. SEM image of a cross-section of a 50nm gate length T-gate, fabricated by digital etching techniques developed at the Ultrafast Systems Group, Dept. of Electronics & Electrical Engineering, University of Glasgow.

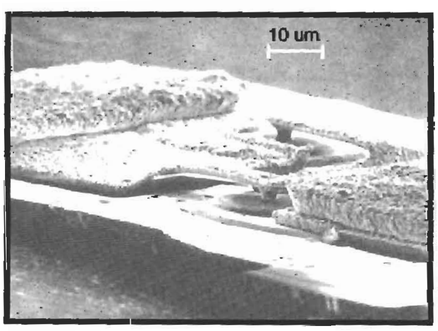


Figure 5. Etching technology for MEMS is under investigation at Technical University, Darmstadt. This SEM image shows an antiparallel structure implemented in III-Vs using etch processing. Such a device is a typical filter for frequencies near 0.6GHz

nique for the gate recess of InP HEMTs. InP-based InGaAs/InAlAs HEMTs are considered to be one of the most promising devices for next generation mm-wave and optical communications because of their superior high frequency and low noise performance.

"We have achieved not only precise etch depth, but also well-controlled undercut width plus the etched surface is very smooth," he says. "We have fabricated 120nm gate length InP HEMTs which showed a maximum transconductance of 600mS/mm and current cut-off frequency of 175GHz. We estimate this performance equals the best results we have achieved using other gate recess techniques."

"For the InP HEMTs, gate recess etching is the most crucial process because the gate recess structure fundamentally determines both performance and uniformity of the devices," he adds. The most widely used gate recess process is selective etching and many studies of selective dry or wet etching for InGaAs over InAlAs have been reported. "By using selective recess etching, the distance between gate and channel - which is crucial to device performance - is solely dependent on the thickness of the InAlAs layer. This should improve flexibility of device design and process control."

MEMS & MOEMS

Etch processing is one of the key technology tools for the fabrication of MEMS, especially those incorporating opto functions. Optical switching represents just one of the growing application areas for III-V MEMS. The use of III-Vs in MEMS and MOEMS addresses a number of problems which appear when using silicon materials. In fact III-Vs are more robust than people think. They are more than robust enough for MEMS because they can be stronger than high quality steel. Moreover, they exhibit useful properties, such as piezoelectricity, and optical functions can be directly incorporate into mechanical structures. Plus, from the processing standpoint, they have a very rich chemistry, so etching techniques can readily be used in the fabrication of MEMS and MOEMS structures.

"The approach chosen by Sandia was to etch AlGaAs epilayers with a sacrificial HF-based chemistry. However, InGaP is also attractive for sacrificial layers owing to the relative inertness," said Olga Blum Spahn. The group has developed a range of devices - including the 1x2 waveguide switch shown in Figure 2 - which have applications that include spaceborne array antennas. With Sandia National Laboratories in Albuquerque, NM, for ten years, Spahn's research interests include microlens fabrication and integration with VCSELs. She is currently working on 1.3 - 1.55μm VCSELs, integration of VCSELs with microsystems (particularly MEMS and LIGA) and MEMS post-processing.

Factors which are the current preoccupation of the etch industry are:

- Smaller footprint equipment
- More efficient processes
- Flexibility in terms of etch chemistry
- Integrated processing
- Single-wafer processing
- Automated handling
- Larger wafers
- Wafer clamping
- Lower maintenance
- Guaranteed process specification
- Lower total cost-of-ownership

Etching technology for MEMS is under investigation at the Technical University of Darmstadt. "For the mm-wave or THz region, the losses for GaAs and in particular for silicon are significant," says Prof. Hans Hartnagel. "The substrate has to be removed by multiple lithography and etch steps. This can involve both dry and wet etching processes. The last etch process being terminated by an epitaxially in-built etch stop layer, like GaAlAs, of only a few monolayers thickness."

Thus it presents considerable challenge, and as he cautions, to optimise all of the many process steps involved in such a device requires a systematic approach: "The experience of the particular technology laboratory staff is invaluable."

Conclusion

The contribution of etching technology to the development and commercialisation of III-V devices is considerable. These examples of some of the important R&D around the world illustrate that by no means is etch processing fully understood. The advent of new materials and structures like GaN and MOEMS require new processes. How successful these become as commercial components hinges on the perfection of reproducible etch processes.